## REMARKS

Claims 1, 2, 4, 5 and 7-52 are pending, with claims 1, 2, 4, 7, 17, 27, 37, 47, 49, and 51 being independent. Claims 17-46 have been withdrawn and claims 3, 6 and 53 have been canceled, leaving claims 1, 2, 4, 5, 7-16 and 47-52 (including independent claims 1, 2, 4, 7, 47, 49 and 51) under consideration. Claims 1, 2, 4, 47, 49 and 51 have been amended. Support for the amendments is discussed below. No new matter has been introduced.

Applicant acknowledges with appreciation the Examiner's allowance of claims 7-16.

Claims 1, 2 and 4 have been rejected under section 112, first paragraph, and claims 1, 2, 4, 5 and 47-52 have been rejected under section 112, second paragraph. Applicant requests reconsideration and withdrawal of these rejections because, as discussed below, the independent claims (as amended) are clear and supported by the specification.

Claims 1, 2 and 4 have been amended to eliminate the references to "a driving period", "a precharge period" and "a programming period" that the Examiner indicated were not supported by the specification. Each of claims 1, 2 and 4 now recites a circuit that either feeds a first current to the transistor so that the gate terminal of the transistor has a first potential, or feeds a second current to the transistor so that the gate terminal of the transistor has a second potential. Support for these features of the claims may be found in Figs. 2 and 3. In particular, Fig. 2 may be said to show the "first current" flowing through the drain-source of the transistor (101) such that the gate terminal (117) of the transistor has "a first potential"; and Fig. 3 may be said to show the "second current" flowing through the drain-source of the transistor such that the gate terminal has "a second potential."

Claim 1, 2 and 4 also have been amended to recite that the transistor feeds the second current to a load (claim 1) or a display element (claim 2), or that the transistor feeds a third current to the load (claim 4). This current flow is shown in Fig. 4 by the current that is fed to the load (109) and corresponds to the recited "second current" or "third current."

Accordingly, claims 1, 2 and 4 are clear and are supported by the specification, and the rejections of those claims and claim 5 (which depends from claim 4) should be withdrawn.

Claim 51 similarly recites a second current source that feeds a first current to the transistor so that the gate terminal of the transistor has a first potential, a first current source that

feeds a second current to the transistor so that the gate terminal of the transistor has a second potential, and that the transistor feeds the second current to the load. The first and second current sources correspond, for example, to the current sources 108 and 115 of Figs. 2-4. Accordingly, the rejection of claim 51 and its dependent claim 52 also should be withdrawn.

Claims 47 and 49 have been amended to eliminate the language that the Examiner found objectionable and to recite feeding a first current to a transistor so that a gate terminal of the transistor has a first potential, feeding a second current to the transistor so that the gate terminal of the transistor has a second potential, and feeding a second or third current to a load through the transistor while the gate terminal of the transistor is kept at the second potential. This arrangement is also shown, for example, in Figs. 2-4. In Fig. 2, a first current (as shown by the arrow) flows to a transistor (101) so that a gate terminal (117) of the transistor has a first potential. In Fig. 3, a second current (as shown by the arrow) flows to the transistor (101) so that the gate terminal (117) of the transistor has a second potential. In Fig. 4, a second current or a third current (as shown by the arrow) flows to a load (109) through the transistor (101) while the gate terminal (117) of the transistor is kept at the second potential. Accordingly, for at least these reasons, claims 47 and 49 are clear and the rejection of claims 47 and 49, and their dependent claims 48 and 50, should be withdrawn.

Claims 1-4 and 47-51 also have been rejected as being anticipated by Herrera (U.S. Patent No. 6,525,574), and claims 5, 6 and 52 have been rejected as being unpatentable over Herrera. Applicant requests reconsideration and withdrawal of these rejections because Herrera does not describe or suggest a circuit that feeds either a first current to the transistor so that the gate terminal of the transistor has a first potential or a second current to the transistor so that the gate terminal of the transistor has a second potential, as recited in claims 1, 2, and 4; feeding a first current to a transistor so that a gate terminal of the transistor has a first potential, and feeding a second current to a transistor so that the gate terminal of the transistor has a second potential, as recited in claims 47 and 49; or first and second current sources that feed currents to a transistor so that the gate terminal of the transistor has a first or a second potential, as recited in claim 51.

While the rejection indicates that the claimed arrangements are shown in Herrera's Figs. 3a and 3b, these figures show an arrangement in which a bias source (Vbias) feeds a voltage to a

gate terminal of a transistor (300). Since the bias source (Vbias) is not a current source and does not feed a current that causes the potential of the gate terminal to assume a particular value, Herrera does not meet the noted features of the claims. Accordingly, for at least this reason, the rejections based on Herrera should be withdrawn.

Applicant submits that all claims are in condition for allowance.

The fee in the amount of $120 for payment of a one-month extension of time is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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